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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,419	03/26/2004	Lahir Shaik Adam	TI-36390	8933
23494	7590	10/31/2005	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED			DANG, PHUC T	
P O BOX 655474, M/S 3999			ART UNIT	
DALLAS, TX 75265			PAPER NUMBER	
			2818	

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

<b>Office Action Summary</b>	Application No. 10/810,419	Applicant(s) ADAM ET AL.	
	Examiner PHUC T. DANG	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on amendment filed September 19, 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-25 is/are pending in the application.  
     4a) Of the above claim(s) 18-25 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-17 is/are allowed.
- 6) ☒ Claim(s) 1-5.7 and 8 is/are rejected.
- 7) ☒ Claim(s) 6 and 9 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>072505</u> . | 6) <input type="checkbox"/> Other: _____  |

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## **DETAILED ACTION**

### **Response to Arguments**

1. Applicant's arguments filed on September 19, 2005 with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

### **Information Disclosure Statement**

2. The office acknowledges receipt of the following items from the applicant:

Information Disclosure Statement (IDS) filed on July 25, 2005.

### **Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-5 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kirkpatrick et al. (U.S. Publication No. US 2004/0266113 A1) in view of Higashitani et al. (U.S. Patent No. 6,159,795).

Regarding claims 1, Kirkpatrick et al. discloses a method of manufacturing a dual gate semiconductor device comprising:

forming a high voltage gate dielectric layer (330, Fig. 3A) over a semiconductor substrate (310, Fig. 3A);

implanting a low dose of nitrogen (332, Fig. 3B) into the semiconductor substrate (310, Fig. 3B) in a low voltage core region (325, Fig. 3B) [see paragraph [0036]-[0041]].

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Kirkpatrick et al. discloses all the features of the claimed invention as discussed above, but does not disclose forming a low voltage core gate dielectric layer over the low voltage core region including forming an intermediate core gate dielectric layer over an intermediate core region.

Higashitani et al., however, discloses forming a low voltage core gate dielectric layer (21, Fig. 1) over the low voltage core region (16, Fig. 1), including forming an intermediate core gate dielectric layer (20, Fig. 1) over an intermediate core region (18, Fig. 1).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above teaching of Kirkpatrick et al. as taught by Higashitani et al. for a purpose of improving a process.

Regarding claims 4, Kirkpatrick et al. discloses the thickness of the gate dielectric layers are applied in the process [0027].

Regarding claim 8, Kirkpatrick et al. discloses forming a first gate over the high voltage gate dielectric layer 455, forming a second gate over the low voltage core gate dielectric layer 435 and forming a third gate over the intermediate core dielectric layer [Fig. 4].

4. Kirkpatrick et al. discloses the claimed invention except for the process parameters as claimed in claims 2-3, 5 and 7. However, the selection of the claimed process parameters would have been obvious to one having ordinary skill in the art at the time the invention was made to improve the process, since it is well settle that when the general conditions of a claim are discloses in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

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### **Allowable Subject Matter**

5. Claims 10-17 would be allowed.

The following is a statement of reason for the indication of allowable subject matter:

Claims 10-17 are considered allowable since the prior art of record and the considered pertinent to the applicant's disclosure does not teach or suggest the claimed invention having a step of forming interconnects extending through dielectric layers located over first, second, and third transistor gates to interconnect the first, second and third transistor gates to form an operative tri-gate integrated circuit as cited in claim 10.

Claims 6 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

None of the Prior art of record teaches or suggests forming the low voltage gate dielectric layer and the intermediate core dielectric layer is conducted in the presence of an environment containing nitrogen as cited in claim 6 and forming the second gate includes forming the second gate such that a concentration of nitrogen within the second gate is substantially uniform through the second gate as cited in claim 9.

### **Conclusion**

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is (571) 272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.

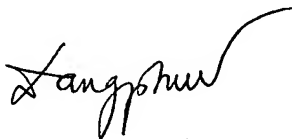
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7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and After Final communications.

8. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Phuc T. Dang

PD

A handwritten signature in black ink, appearing to read 'Phuc T. Dang', with a long, sweeping horizontal stroke extending to the right.

Primary Examiner

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